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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,227	06/24/2003	Mohammad Nejad	BP 2512	1088

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EXAMINER	
SINKANTARAKORN, PAWARIS	
ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/602,227	NEJAD ET AL.	
	Examiner	Art Unit	
	Pao Sinkantarakorn	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-27,29-32,37,38,41 and 42* is/are rejected.

7)☒ Claim(s) *6-8,28,33-36,39,40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 6/20/2007 have been received and made of record.

2. Claims 1-42 are pending.

Claim Rejections - 35 USC § 103

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-5, 9, 11, 14-18, 22, 24, 27, 29-32, 38, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramoto et al. (US 6,657,953) in view of Graves (US 4,667,324).

Hiramoto et al. disclose, **regarding claims 1, 14, 27, 41**, an upstream multiplexing integrated circuit within a multistage bit stream multiplexer/a method (see column 4 line 1) comprising:

a second multiplexing integrated circuit that receives the second plurality of bit streams and that outputs at least one high-speed bit stream at a line bit rate that exceeds the second bit rate (see column 4 lines 1-5, multiplexing between DS1 signals and DS3 signals, wherein DS1 signals have a lower speed than that of DS3 signals);

a clock circuit (see column 4 line 26), wherein the clock circuit generates a forward transmit clock for use by the first multiplexing integrated circuit (see column 4 lines 27-29) in producing the second plurality of bit streams (see column 4 lines 1-5, producing DS3 signals) based upon a reference clock signal selectable from a plurality of inputs (see column4 lines 30), wherein the inputs include a reverse transmit clock generated by the second multiplexing integrated circuit (see figure 1, a line starting from Loopback Control Unit and ending at Clock Generation Unit, the loopback signal is used to adjust the clock circuit).

Hiramoto et al. disclose all the claimed limitations except another stage of multiplexing circuit, wherein the circuit multiplexes PCM signals into DS1 signals. The invention of Graves from the same or similar fields of endeavor discloses a multistage

multiplexer, wherein the first multiplexing circuit receives the first plurality of inputs at a first bit rate (see figure 1, input signals CH1-CH24 of M1) and that produces a second plurality of bit streams at a second bit rate (see figure 1, output signals DS-1 of M1), wherein the first plurality of bit streams are greater in number than the second plurality of bit streams are in number (see figure 1, 24 input signals CH1-CH24 and 1 output signal DS-1 at M1), and wherein the first bit rate is less than the second bit rate (see figure 1, CH1-CH24 signals are DS0 signals, which has slower rate than the output DS1 signal).

Thus, it would have been obvious to the person of ordinary skill in the art to implement the first stage of the multiplexing circuit as taught by Grave into the multiplexing circuit of Hiramoto et al. by implementing a first stage multiplexing circuit, wherein the first stage multiplexing circuit takes in DS0 signals and produce DS1 signals to be passed on to the second stage multiplexing circuit.

The motivation for implementing the first stage of the multiplexing circuit into the multiplexing circuit is that it allows the circuit to convert the rate from a lower rate to a high-speed bit stream. A 2-stage multiplexing circuit allows the input rate to be DS0 rate, and the output rate to be DS3 rate, instead of DS0 rate to DS1 rate of 1-stage multiplexing circuit.

Hiramoto et al. in view of Grave disclose, **regarding claims 2, 15, 29**, disclose all the subject matter of the claimed limitations except a communication ASIC from which the first multiplexing integrated circuit receives the first plurality of bit streams; and a media interface that receives the at least one high-speed bit stream and produces

a media output. However, it is well known to the person of ordinary skill in the art to have a multiplexing circuit receive plurality of input signals from a signal source, such as ASIC, and produce output streams to be transmitted to a media interface to produce a media output.

Thus, it would have been obvious to the person of ordinary skill in the art to implement a multiplexing circuit, wherein the signal source is a communication ASIC, and the output signals are transmitted to the media interface to produce a media output into the multistage multiplexing circuit of as taught by Hiramto et al. in view of Grave.

The motivation for implementing a multiplexing circuit, wherein the signal source is a communication ASIC, and the output signals are transmitted to the media interface to produce a media output is that ASIC provides better performance for media transmission.

Regarding claims 3, 16, 30, wherein the plurality of inputs further comprises an external oscillator output (see column 4 lines 30-32);

regarding claims 4, 17, 31, wherein the plurality of inputs further comprises a voltage controlled oscillator output (see figure 2 reference numeral 17-3);

regarding claims 5, 18, 32, wherein the reference clock signal is selected based upon a clock selector input (see figure 2 reference numeral 17-2);

regarding claims 9, 22, wherein the forward transmit clock is a source centered doube data rate clock with respect to each of the plurality of second bit streams (see column 13 lines 19-21, VCXO is used to oscillate the forward transmit clock)

regarding claims 11, 24, 38, wherein the first multiplexing integrated circuit generates the reverse clock based on an external oscillator reference clock (see column 13 lines 19-25).

regarding claim 12, wherein the first multiplexing integrated circuit further comprises a phase detector that receives a first input from a loop timing circuit and a second input from one of the plurality of inputs (see column 13 lines 22-26).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramoto et al. in view of Graves as applied to claim 1 above, and further in view of Metz et al. (US 4,360,912).

Hiramoto et al. in view of Graves disclose all the subject matter of the claimed limitations except the first multiplexing integrated circuit comprises integrated circuits formed on a silicon substrate and the second multiplexing integrated circuit comprises a substrate selected from the group consisting of InP, SiGe, GaN, GaAs, and Si. However, Metz et al. from the same or similar fields of endeavor disclose a multiplexer which is comprised of CMOS parts (see column 6 lines 38-41, CMOS is comprised of Silicon Si).

Thus, it would have been obvious to the person of ordinary skill in the art to use a multiplexer that is comprised of CMOS parts as taught by Metz et al. in the multistage multiplexing integrated circuit of Hiramoto et al. in view of Graves.

The motivation for using a multiplexer that is comprised of CMOS parts is that CMOS multiplexer makes a faster circuit and less capacitiance.

Allowable Subject Matter

7. Claims 6-8, 28, 33- 36, and 39-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10, 19-21, 23, 25, 37, and 42 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 6/20/2007 have been fully considered but they are not persuasive.

On page 4 of the remarks filed 6/20/2007, the applicant submits that there has not been a prima facie showing that substantiates the rejection of Applicant's claimed invention. There is no suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art to modify the "circuit quality degradation device" of Hiramoto and "the mono-stage multiplexer device" of

Graves to achieve Applicant's claimed invention. The examiner respectfully disagrees. The motivation for implementing multistage multiplexing circuit as taught by Graves into the loopback device of Hiramoto et al. is that it allows the multistage multiplexing circuit to convert the rate of the signals from DS3 to DS1 and then DS1 to DS0, instead of converting the rate of the signals from DS3 to DS1 only. The examiner provides a clear articulation of the reasons why the claimed invention would have been obvious. Therefore, the rejection under 103 is proper. *See KSR, 82 USPQ2d 1385 (2007).*

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pao Sinkantarakorn whose telephone number is 571-

270-1424. The examiner can normally be reached on Monday-Thursday 9:00am-3:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PS

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER